EAST SEARCH

4/15/04

L#	Hits	Search String	Databases
L2	2	6,581,191.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	2	6,618,839.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	473212	(integrated or digital) adj circuit$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	1329	((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	14	((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) w	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	48	((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) s	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	7	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	97	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	7	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	28	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	28	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	16	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	8	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	9	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	9	((((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	6	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	45	((integrated or digital) adj circuit$1) and (debug$4 with (target near2 (environment	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	2	((integrated or digital) adj circuit$1) and (debug$4 with (target near2 environment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	7	((integrated or digital) adj circuit$1) and (debug$4 with (target near2 environment))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	11	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	2	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	2	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	90	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	55	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	113	(((integrated or digital) adj circuit$1) and (HDL near2 (description or describe$1))) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	14	circuit$1) and ((HDL near2 (description or describe$1)) same debug$4)) and (state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	5,937,190.pn. and (control near2 signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	6	and ((HDL near2 (description or describe$1)) same debug$4)) and (signal with (HI	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	17	(((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) :	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

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Results of search set L10:((integrated or digital) adj circuit$1) and ((HDL near2 (description or describe$1)) same debug$4)

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20040025122	A1	Hardware-based HDL code coverage and design analysis	20040205	716/4	
US 20030204831	A1	METHOD AND ARRANGEMENT FOR RAPID SILICON PROTOTYPING	20031030	716/18	
US 20030184339	A1	Integrated circuit device	20031002	326/47	
US 20030182642	A1	Hardware debugging in a hardware description language	20030925	716/4	
US 20030131325	A1	Method and user interface for debugging an electronic system	20030710	716/4	
US 20030093734	A1	Implementation of an assertion check in ATPG models	20030515	714/731	
US 20030093733	A1	Modeling custom scan flops in level sensitive scan design	20030515	714/726	
US 20030070013	A1	Method and apparatus for reducing power consumption in a digital processor	20030410	710/59	
US 20030069724	A1	Method and system for debugging an electronic system using instrumentation circ	20030410	703/16	
US 20030023941	A1	Computer-aided design system to automate scan synthesis at register-transfer lev	20030130	716/4	
US 20020171449	A1	Test system and manufacturing of semiconductor device	20021121	324/765	
US 20020138801	A1	Method and apparatus for diagnosing failures in an integrated circuit using design-	20020926	714/729	
US 20020129334	A1	Interface based design using a tabular paradigm	20020912	717/123	
US 20020123875	A1	Hierarchical processing of simulation model events	20020905	703/17	
US 20020052729	A1	Apparatus and method for verifying a logic function of a semiconductor chip	20020502	703/28	
US 20020002698	A1	Method for verifying the design of a microprocessor	20020103	716/4	
US 20010049593	A1	Software tool to allow field programmable system level devices	20011206	703/14	
US 20010022743	A1	Semiconductor integrated circuit device	20010920	365/189.03	
US 20010021558	A1	Semiconductor integrated circuit device	20010913	438/286	
US 20010003841	A1	Dual rom microprogrammable microcontroller and universal serial bus microcontro	20010614	712/211	
US 6665855	B2	Method and arrangement for rapid silicon prototyping	20031216	716/18	
US 6618839	B1	Method and system for providing an electronic system design with enhanced debu	20030909	716/4	
US 6601218	B2	Semiconductor integrated circuit device	20030729	716/1	
US 6581191	B1	Hardware debugging in a hardware description language	20030617	716/4	
US 6523151	B2	Method for verifying the design of a microprocessor	20030218	716/4	
US 6470475	B2	Synthesizable synchronous static RAM	20021022	716/1	
US 6467010	B1	Method and arrangement for passing data between a reference chip and an exterr	20021015	710/305	
US 6436741	B2	Semiconductor integrated circuit device	20020820	438/149	
US 6400173	B1	Test system and manufacturing of semiconductor device	20020604	324/765	
US 6370635	B2	Dual ROM microprogrammable microcontroller and universal serial bus microcontr	20020409	712/32	
US 6353906	B1	Testing synchronization circuitry using digital simulation	20020305	714/741	
US 6347395	B1	Method and arrangement for rapid silicon prototyping	20020212	716/18	
US 6338109	B1	Microcontroller development system and applications thereof for development of a	20020108	710/310	
US 6272451	B1	Software tool to allow field programmable system level devices	20010807	703/13	
US 6266630	B1	Method and apparatus for providing a graphical user interface for simulating desig	20010724	703/14	

US 6154803 A	Method and arrangement for passing data between a reference chip and an exterr	20001128	710/310
US 6132109 A	Architecture and methods for a hardware description language source level debug	20001017	717/131
US 6041371 A	Asynchronous input/output for integrated circuits that latches external asynchronou	20000321	710/58
US 5937190 A	Architecture and methods for a hardware description language source level analys	19990810	717/131
US 5920711 A	System for frame-based protocol, graphical capture, synthesis, analysis, and simul	19990706	703/15
US 5911059 A	Method and apparatus for testing software	19990608	703/23
US 5859993 A	Dual ROM microprogrammable microprocessor and universal serial bus microcont	19990112	712/208
US 5841663 A	Apparatus and method for synthesizing integrated circuits using parameterized HD	19981124	716/18
US 5519627 A	Datapath synthesis method and apparatus utilizing a structured cell library	19960521	716/18
US 6618839 B	Fabricated integrated circuit debugging method e.g. for application specific integra	20030909	
US 20030131325 A	Fabricated integrated circuits debugging method for electronic system designs, inv	20030710	
US 20030069724 A	Computer system debugging method involves translating debug data received fron	20030410	
WO 200140941 A	Hardware debugging system for debugging electronic system containing electronic	20010607	